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APPLICATION
FOR
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LETTERS PATENT

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FOR: ELASTIC STORE CIRCUIT

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ELASTIC STORE CIRCUIT

BACKGROUND OF THE INVENTION

1.   Field of the Invention

The present invention relates to an elastic store circuit

5   for absorbing the propagation delay time difference among

plural pieces of data transmitted through different

transmission lines.

2.   Description of the Related Prior Art

For example, assume that optical fiber capable of

10   transmitting data of a maximum of 2.4 Gbps is used in a section

of an optical fiber transmission line through which data of

10 Gbps is transmitted.   First, data of 10 Gbps is divided

into four pieces of data of 2.4 Gbps, and then the data of

10 Gbps is to be restored from the four pieces of data of 2.4

15   Gbps.   If the four pieces of data of 2.4 Gbps are transmitted

through different transmission lines, then there arise

propagation time differences among the four pieces of data

based on the variance of each transmission line.   In this case,

an elastic store circuit is required to absorb the propagation

20   delay time difference.

FIG. 1 shows an example of a public elastic store circuit.

The circuit includes a clock selector 4, a frame pulse retiming

circuit 8, four frame counters 9, a detection circuit 10, and

a read address counter 7.   The data of 2.4 Gbps transmitted

25   through four transmission lines are converted from optical

signals to electric signals, and provided with clock and frame pulses. Since these four pieces of data of 2.4 Gbps are asynchronous to one another, it is necessary for the elastic store circuit to set these pieces of data in a synchronous

5   state.

The operation of the circuit shown in FIG. 1 is described below. The clock selector 4 optionally selects a read clock of elastic store memory 6 from among the four asynchronous clocks. The frame pulse retiming circuit 8 retimes the four

10   frame pulses indicating the MSB (most significant bit) by the read clock optionally selected by the clock selector 4. The retiming operations are completely asynchronous. The frame pulse after the retiming operation is used as a load pulse of the frame counter 9. Each of the frame counters 9 is

15   initialized in the receipt order of the frame pulses, and each frame counter 9 starts counting data of 2.4 Gbps by the clock selected by the clock selector 4. The detection circuit 10 compares the count values of the four frame counters, and determines that the data having the minimum count value for

20   a predetermined time is the data of 2.4 Gbps which arrived last. The output based on the determination result is a load pulse of the read address counter 7 of the elastic store memory 6. Therefore, the read phase of the elastic store memory 6 is determined based on the data of 2.4 Gbps having the longest

25   propagation delay time. As a result, the propagation delay time differences among the four pieces of data of 2.4 Gbps

are absorbed, thereby successfully restoring the data of 10 Gbps.

However, the above mentioned elastic store circuit includes, for example, four frame counters for counting one frame (125 μ sec) of the SONET/SDH frame format, and compares the count values of the respective frame counters. Therefore, the circuit is complicated and large, and requires large power consumption. Furthermore, the circuit retimes four asynchronous frame pulses using one clock so as to realize the synchronous operations of four pieces of data of 2.4 Gbps. However, the frame pulse is normally a single pulse of 1 clock width. When the retiming phases for retiming frame pulses are asynchronous to one another, the output of the retiming flip-flop circuit falls in a metastable state, and the frame pulses having a single clock width are not correctly retimed.

SUMMARY OF THE INVENTION

Therefore, the present invention aims at providing an elastic store circuit and a data receiving method capable of reducing the circuit size and the power consumption by simplifying the detection unit for detecting the receipt of data having the longest propagation delay time, and also detecting correct data.

To attain the above mentioned object, the elastic store circuit according to the present invention includes: a clock selector for selecting a read clock from a plurality of clocks; a data receipt detection circuit for detecting plural pieces

of received data; a longest delay data detection circuit for detecting data having the longest propagation delay time; and a reset circuit for receiving the output from the longest delay data signal detection circuit and a read clock, and
5   transmitting a reset signal to the data receipt detection circuit and a read address counter of the elastic store memory. The reset signal can be transmitted to the data receipt detection circuit through the read address counter of the elastic store memory. The longest delay data signal detection
10   circuit can use an AND circuit for inputting each output signal of the data receipt detection circuit.

The data receiving method according to the present invention includes the steps of: receiving data from a plurality of transmission lines and storing the data in the
15   elastic store memory, receiving a clock and frame pulse corresponding the data, selecting one read clock from a plurality of clocks, receiving a frame pulse by the AND circuit and detecting the last received data, and reading the data from each elastic store memory according to the signal based
20   on the output from the AND circuit and the read clock.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and advantages of the present invention will become apparent from the following detailed description when taken with the accompanying drawings
25   in which:

FIG. 1 shows an example of a conventional elastic store circuit;

FIG. 2 is a block diagram of an example of the elastic store circuit according to the present invention;

FIG. 3 is a block diagram of an example of the elastic store circuit according to the present invention; and

FIG. 4 is a block diagram of a more detailed example of the elastic store circuit according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

By referring to FIG. 2, the elastic store circuit of the first example comprises: the clock selector 4 for selecting one clock from among four input clocks (CLK#1 - #4); and a data receipt detection circuit 1 for inputting four frame pulses (WFP#1 - #4). Furthermore, the elastic store circuit also comprises: a longest delay data detection circuit 2 for receiving data receipt information from the data receipt detection circuit 1; and a reset circuit 3 for receiving output of each of the longest delay data detection circuit 2 and the clock selector 4, and outputting a reset pulse. The reset pulse is transmitted to a read address counter 7 and the data receipt detection circuit 1.

According to the second example, by referring to FIG. 3, the reset pulse is output from the reset circuit 3 to the data receipt detection circuit 1 through the read address counter 7

In the above mentioned elastic store circuit, the clock selected by the clock selector 4 from the clocks (CLK#1 – #4) is transmitted to the reset circuit 3, the read address counter 7, and the elastic store memory 6. The read address counter 7 receives the reset pulse.

FIG. 4 shows a detailed example of the central portion of the elastic store circuit shown in FIG. 2. The data receipt detection circuit 1 comprises four set/reset flip-flop circuits 1-1, 1-2, 1-3, and 1-4. The frame pulses (WFP#1 – #4) corresponding to the data signals are respectively input into the set input terminals of the flip-flop circuits 1-1, 1-2, 1-3, and 1-4. The reset input terminals of the flip-flop circuits receive the reset pulses output by the reset circuit 3 or the read address counter 7. The longest delay data detection circuit 2 comprises a 4-input AND circuit for receiving the output of the above mentioned four flip-flop circuits. The reset circuit 3 comprises a flip-flop circuit 3-1 for receiving an output signal of the 4-input AND circuit, and two flip-flop circuits 3-2 and 3-3 serially connected to the flip-flop circuit 3-1. These three flip-flop circuits configure a shift register. The clock signal selected by the clock selector 4 is input into these flip-flop circuits. The reset circuit 3 comprises a 2-input AND circuit 3-4 for receiving an input signal and an output signal of the flip-flop circuit 3-3, and outputting a reset signal.

Described below are the operations of the elastic store circuit. Four pieces of data (W data #1 – #4) of 2.4 Gbps

are input into the elastic store memory 6 respectively. The clocks (CLK#1 - #4) and the frame pulses (WFP#1 - #4) added to each piece of data #1 - #4 are similarly input into the elastic store memory 6 and a write address counter 5. In

5   addition, when the data #1 of 2.4 Gbps is input into the elastic store memory 6, the frame pulse WFP#1 is input into the set terminal of the set/reset flip-flop circuit 1-1. When the frame pulse WFP#1 is input, the set/reset flip-flop circuit 1-1 outputs an H signal. Upon receipt of the frame pulses

10 WFP#2 - #4, the set/reset flip-flop circuits 1-2, 1-3, and 1-4 similarly output an H signal. When these flip-flop circuits are set, they continue outputting H signals until they receive reset signals. Therefore, when data receipt is detected, these flip-flop circuits have to be reset. When

15 the 4-input AND circuit (longest delay data detection circuit 2) receives all the four H signals (that is, when it receives the data signal having the longest propagation delay time), the circuit changes the output from the L signal to the H signal. The shift register in the reset circuit 3 (that is, the flip-flop

20 circuits 3-1, 3-2, and 3-3) retimes the change from the L signal to the H signal using the clock selected by the clock selector 4. The 2-input AND circuit 3-4 receives input and output signals of the flip-flop circuit 3-3, and generates a differential pulse having one clock width. When the

25 differential pulse is input as a load pulse into the read address counter 7 of the elastic store memory 6, the read address counter 7 is loaded with the count value of 0, and reset. When the

read address counter 7 is initialized, the reading timing of the elastic store memory 6 is in synchronization with the last received data. Therefore, based on the data of 2.4 Gbps having the longest propagation delay time, the read phase of the

5   elastic store memory 6 is determined. As a result, the data (R data #1 - #4) of 2.4 Gbps and the frame pulses (RFP#1 - #4) are output from the four elastic store memory units 6 at the same timing. The above mentioned differential pulse or the output of the read address counter 7 are used as reset

10   pulses of the set/reset flip-flop circuits 1-1, 1-2, 1-3, and 1-4 of the data receipt detection circuit 1.

As described above, the elastic store circuit according to the present invention detects the order of receiving a plurality of data signals having different propagation delay

15   times by a plurality of set/reset flip-flop circuits and the 4-input AND circuit. Therefore, the circuit has a configuration simpler than that of the conventional circuit, and can detect a received data signal having the longest propagation delay time without fail. Furthermore, the

20   circuit according to the present invention converts the receipt of the data having the longest propagation delay time in the plurality of data signals into an H pulse signal, and a coincident result is retimed, thereby easily performing synchronous operations among plural pieces of asynchronous

25   data.

While the present invention has been described in connection with certain preferred embodiments, it is to be

understood that the subject matter encompassed by the present invention is not limited to those specific embodiments. On the contrary, it is intended to include all alternatives, modifications, and equivalents as can be included within the

5   spirit and scope of the following claims.